PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
PCT3144		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/JP 01/06230	18/07/2001	21/07/2000
Applicant		
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readble form.

[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

[X] the text is approved as submitted by the applicant.

[ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

[ ] the text is approved as submitted by the applicant.

[X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

[X] as suggested by the applicant.

[ ] because the applicant failed to suggest a figure.

[ ] because this figure better characterizes the invention.

[ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP 01/06230

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

According to the present invention, when a semiconductor element (7) having protruding electrodes (5) formed thereon is connected to a circuit board (1) via conductive resin (6), stable connection is made even when an electrode pitch is small on the semiconductor element (7). On semiconductor element package regions on the circuit board (1), a paste electrode material (2) containing photopolymerizable materials is printed to form a film having a prescribed thickness, and this electrode material film (2) is baked after exposure and development thereof so as to obtain circuit electrode (4) s having edges warped in a direction of going apart from the circuit board (1) surface. Then, the protruding electrodes (5) and the concave surfaces of the circuit electrodes (4) are brought in abutment with each other and connected via the conductive resin (6) which surrounds the abutments between the respective electrodes (4, 5) and is held on the concave surfaces of the circuit electrodes (4). With this arrangement, the concave surfaces of the circuit electrodes (4) act as saucers and prevent the conductive resin (6) from being squeezed out, thereby eliminating possible occurrence of short circuits.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 01/06230

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/11 H05K3/32 H05K3/06 . H05K1/09 H01L21/48
H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 049 480 A (NEBE ET AL.) 17 September 1991 (1991-09-17) column 12, line 30 -column 13, line 4 ---	1,2,5,6
A	EP 0 657 932 A (MATSUSHITA ELECTRIC IND CO LTD) 14 June 1995 (1995-06-14) column 9, line 2 - line 37; figure 1 ---	1,5,6
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 12, 26 December 1996 (1996-12-26) & JP 08 222840 A (SUMITOMO METAL IND LTD;SUMITOMO KINZOKU ELECTRO DEVICE:KK), 30 August 1996 (1996-08-30) abstract --- -/--	1,4-6

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2002	02/04/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Mes, L

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Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 09, 30 July 1999 (1999-07-30) & JP 11 121527 A (PFU LTD), 30 April 1999 (1999-04-30) abstract	1,5,6
A	US 5 338 391 A (SUPPELSA ET AL.) 16 August 1994 (1994-08-16) abstract; figures	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 01/06230

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5049480 A	17-09-1991	NONE	
EP 0657932 A	14-06-1995	CN 1113607 A ,B	20-12-1995
		CN 1221309 A	30-06-1999
		DE 69428181 D1	11-10-2001
		EP 0657932 A2	14-06-1995
		JP 7231050 A	29-08-1995
		US 5640051 A	17-06-1997
		US 5628919 A	13-05-1997
JP 08222840 A	30-08-1996	NONE	
JP 11121527 A	30-04-1999	NONE	
US 5338391 A	16-08-1994	NONE	

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 08222840
PUBLICATION DATE : 30-08-96

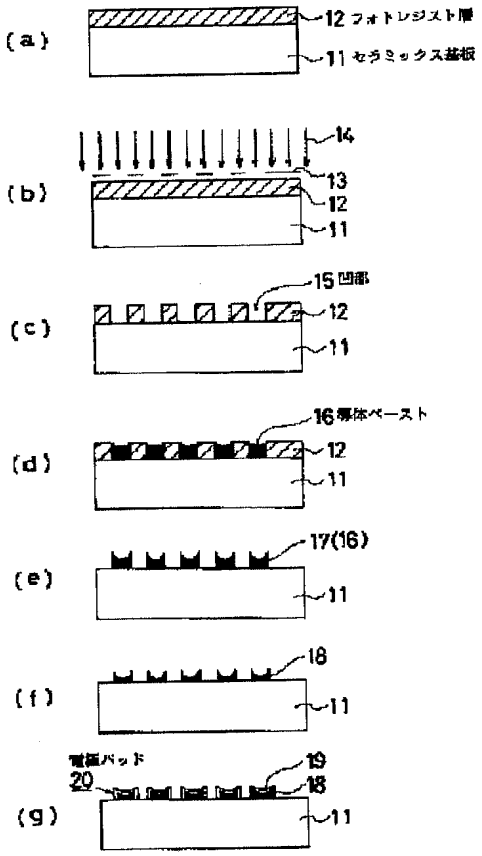
APPLICATION DATE : 15-02-95
APPLICATION NUMBER : 07026583

APPLICANT : SUMITOMO KINZOKU ELECTRO DEVICE:KK;

INVENTOR : TANAKA KAZUNARI;

INT.CL. : H05K 3/34 H05K 3/10

TITLE : CIRCUIT BOARD WITH ELECTRODE PAD AND ITS MANUFACTURE



ABSTRACT : PURPOSE: To improve the adhesion between solder bumps and electrode pads to prevent insufficient connection even when a large heat cycle load acts on the bumps or pads by specifying the size of the central recessed sections of the pads.

CONSTITUTION: After a photoresist layer 12 is formed over the entire surface of a ceramic substrate 11, recessed sections 15 ≥3μm deep are formed on the layer 12 in an electrode pad forming pattern 18 and filled with conductor paste 16. Then only the dried bodies 17 of the conductor paste are left on the substrate 11 and the pattern 18 is formed by baking the dried bodies 17. After forming the pattern 18, electroless-plated layers 19 are formed as electrode pads 20. Finally, an LSI is connected to the substrate 11 through the pads 20 and conducted.

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 11121527
PUBLICATION DATE : 30-04-99

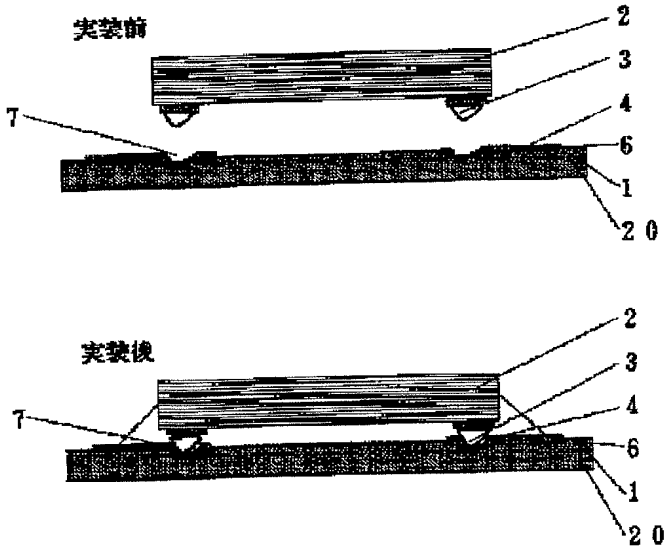
APPLICATION DATE : 21-10-97
APPLICATION NUMBER : 09287491

APPLICANT : PFU LTD;

INVENTOR : SENKAWA YASUHIDE;

INT.CL. : H01L 21/60 B28B 3/02 H05K 1/18

TITLE : MOUNTING OF BARE CHIP COMPONENT, MANUFACTURE OF CERAMIC BOARD, THE CERAMIC BOARD AND SEMICONDUCTOR DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To connect parts, which are connected with bumps of conductors with the bumps in three dimensions to enlarge engaging effect of the bumps into the conductors and the contact area of the bumps with the conductors and to avoid the generation of defects in a bare chip component due to sliding of the connection parts of the bare chip component with a ceramic board, by a method wherein the parts, which are connected with the bumps under the lower part of the bare chip component of the conductors on the ceramic board are formed, in such a way that the surface of the ceramic board is formed into a recessed form.

SOLUTION: Parts, which are connected with bumps 3 under the lower part of a bare chip component 2, of conductors 4 on a ceramic board 1 are constituted in recessed parts 7 formed in the surface of the board 1 in such a way that the surface of the board 1 is formed into a recessed form. As a result, parts, which are connected with the bumps 3 under the lower part of the component 2 of the conductors 4 on the board 1 are connected three dimensionally with the bumps 3, the engaging effect of the bumps 3 into the conductors 4 and the contact area of the bumps 3 with the conductors 4 can be enlarged, and the generation of a defect in the component 2 due to sliding of the connection parts of the component 2 with the board 1, which is accompanied by heating/heat generation due to a difference between the thermal expansion coefficients of the component 2 and the board 1, can be avoided. Moreover, a conductor paste, which is a connection medium between the bumps 3 and the conductors 4, can be also dispensed with, a leveling of the bumps 3 is also dispensed with, and the reliability of the connection of the component 1 with the board 1 can be improved.

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WO 02/09485 A2

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(81) Designated States *(national)*: CN, ID, KR, SG, US.

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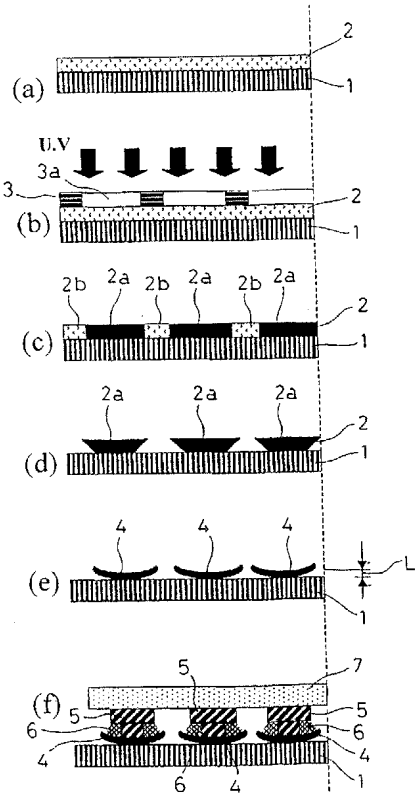
Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FLIP CHIP PACKAGE, CIRCUIT BOARD THEREOF AND PACKAGING METHOD THEREOF



(57) Abstract: According to the present invention, when a semiconductor element having protruding electrodes formed thereon is connected to a circuit board via conductive resin, stable connection is made even when an electrode pitch is small on the semiconductor element. On semiconductor element package regions on the circuit board, a paste electrode material containing photopolymerizable materials is printed to form a film having a prescribed thickness, and this electrode material film is baked after exposure and development thereof so as to obtain circuit electrodes having edges warped in a direction of going apart from the circuit board surface. Then, the protruding electrodes and the concave surfaces of the circuit electrodes are brought in abutment with each other and connected via the conductive resin which surrounds the abutments between the respective electrodes and is held on the concave surfaces of the circuit electrodes. With this arrangement, the concave surfaces of the circuit electrodes act as saucers and prevent the conductive resin from being squeezed out, thereby eliminating possible occurrence of short circuits.

WO 02/09485 A2

DESCRIPTION

FLIP CHIP PACKAGE, CIRCUIT BOARD THEREOF AND PACKAGING METHOD THEREOF

Technical Field

The present invention relates to a flip chip package, a circuit board thereof and a packaging method thereof, and specifically to a flip chip package having an electrode structure suitable for a flip chip package, a circuit board thereof and a packaging method thereof.

Background Art

An electronic circuit has been recently higher in density, and the need for a smaller area and connecting resistance has been intensified regarding a packaged device. One of means for attaining a high-density package is flip chip package. Several kinds of packaging methods are available for the flip chip package, and in consideration of easy repair and unleading, which has attracted attention in recent years, SBB method (Stud Bump Bonding) is a desirable technique. The SBB method is a technique for forming protruding electrodes, which are made of materials such as Au, on a semiconductor element by a wire bonding method and for connecting the protruding electrodes and electrodes on a circuit board via conductive resin.

Referring to FIG. 3, a paste electrode material is firstly printed on a circuit board 11 by a method such as screen printing, and the circuit board 11 is baked at a temperature of sintering the electrode material. Thus, circuit electrodes 12 are formed on the circuit board 11. On the other hand, protruding electrodes 14 are formed on a semiconductor element 13 by a method such as wire bonding, and a layer of conductive resin 15 is formed on the protruding electrodes 14 by transferring and so on. Thereafter, the circuit board

11 and the semiconductor element 13 are positioned high accurately and a suitable load is applied thereon. Hence, the semiconductor element 13 is packaged on the circuit board 11.

However, the above conventional packaging method is disadvantageous as in the following. First, since the semiconductor element 13 has decreased in electrode pitch in recent years, an electrode pitch on the circuit board 11 needs to be smaller accordingly. However, according to the conventional screen printing method, a pitch is limited up to 300 μm and printing is difficult with a pitch below the limit, causing frequent short circuits and breaks in a wire. Consequently, the yields are lowered.

Secondly, when the semiconductor element 13 is smaller in electrode pitch, it is quite difficult to control a quantity of the conductive resin 15 transferred onto the protruding electrodes 14 of the semiconductor element 13. Particularly, short circuits are more likely to occur. In order to prevent the short circuits, a quantity of the conductive resin 15 is set smaller than that of the conventional art. However, since the electrode material expands laterally, the circuit electrodes 12 are each half-round in cross section when an electrode pitch is 100 μm. In the case where flip-chip packaging is carried out on the circuit electrodes 12, the conductive resin 15 is squeezed out of the circuit electrodes 12 as shown in FIG. 3. Therefore, the conductive resin 15, which is squeezed out of the adjacent circuit electrodes 12, may be short-circuited.

Disclosure of Invention

The object of the present invention is to make a stable connection with a circuit board even when a semiconductor element has a small electrode pitch.

In order to solve the foregoing problem, when protruding electrodes formed on the semiconductor element are connected

to circuit electrodes on the circuit board via conductive resin, the present invention comprises the steps:

(a) forming an electrode material film having a prescribed dry film thickness by using a paste electrode material containing a photopolymerizable material;

(b) exposing and developing the electrode material film;

(c) baking the developed electrode material film; and

(d) flip-chip packaging the semiconductor element on the circuit electrodes formed in the above steps.

In the above steps, concave circuit electrodes having warped edges are formed on the circuit board. Since the concave surfaces of the circuit electrodes act as saucers, it is possible to flip-chip package the semiconductor element without squeezing out any conductive resin. Consequently, it is possible to eliminate the occurrence of short circuits, achieving a reliable packaging for the semiconductor element.

Ceramic is applicable as the circuit board. The circuit board can be provided not only with a circuit including circuit electrodes for mounting the above semiconductor element, but also a circuit for mounting components other than the semiconductor element as well as a circuit for making connection with another board.

Such an electrode material is used that contains, at least, metallic materials such as Au, Ag, or Cu and glass as inorganic components, and a monomer and a polymer which also serve as polymeric materials and a photoinitiator as organic components. Ni or Au plating may be applied to the surface of the formed circuit electrodes.

Such a semiconductor element is used that is formed with the protruding electrodes made of metallic materials such as Au, Al, Cu, and solder. Any method including wire bonding and plating is applicable for forming the protruding electrodes.

The conductive resin is applicable as long as the resin contains conductive components such as Au, Ag, and Cu to

connect the protruding electrodes on the semiconductor element and the circuit electrodes on the circuit board. Any type of resin is applicable regardless of whether it is thermosetting or thermoplastic.

In the above step (a), a film is formed by printing a paste electrode material on the circuit board. The electrode material needs to be printed only on a package region for packaging the semiconductor element. The other regions may be formed with a circuit pattern in advance according to the above mentioned conventional method. In addition, upon printing, which is not intended for forming a circuit pattern, printing may be performed over the entire surface of the package region. Thus, a rough printing such as a conventional screen printing is sufficiently applicable. The electrode material is dried at a suitable temperature to prevent the material from flowing after printing. However, a printing plate and printing conditions need be set so as to secure a prescribed film thickness, which is preferably 10 to 20 (μm).

In step (b), a glass mask and so on are positioned on the circuit board, on which the electrode material is printed and dried. The glass mask is formed such that only an electrode region having the semiconductor element transmits light. Ultraviolet rays having a wavelength of 320 to 370 nm are radiated at 300 to 500 mJ. Thereby, polymeric materials on an electrode region which transmits ultraviolet rays are started by a photoinitiator to react and polymerized. After some appropriate time, the board is entirely developed by means of a solution for dissolving a polymeric material which has not reacted. Thus, the film is removed from other parts than the electrode regions and remains on the electrode regions. At this time, by adjusting the film thickness, polymeric materials receiving less light are left to remain insufficiently polymerized toward the board. Upon development, erosion is started from non-electrode regions

from which the film has been removed, further to wider area toward the board. As a result, the film has a trapezoidal cross section on the electrode region. When a film thickness is small, all the polymeric materials are polymerized and it is impossible to obtain a film having a trapezoidal cross section. Therefore, the above film thickness is demanded.

In step (c), the circuit board completed with exposure and development is baked at a temperature for sintering the electrode material, and the circuit electrodes are baked onto the circuit board. At this time, the electrode material film is caused to slightly shrink, so that both ends of the formed circuit electrode are slightly warped (such warped part is called an edge curl) and the cross section of the circuit electrode becomes arc-shaped. Plating of Ni, Au and so on may be applied in order to protect the electrode surfaces after baking.

In step (d), the semiconductor element having the protruding electrodes formed thereon is flip-chip packaged on the circuit board by using the conductive resin. At this time, the edge curl of the circuit electrode acts as a wall, thereby preventing the conductive resin from being squeezed out.

Brief Description of Drawings

FIG. 1 is a process sectional view explaining a method of flip-chip packaging a semiconductor element according to Embodiment 1 of the present invention;

FIG. 2 is a process sectional view explaining a method of flip-chip packaging a semiconductor element according to Embodiment 2 of the present invention; and

FIG. 3 is a process sectional view explaining a conventional method of flip-chip packaging the semiconductor element.

Best Mode for Carrying Out the Invention

The present invention is characterized in that when a semiconductor element is flip-chip packaged on a circuit board by using a conductive resin, the element having protruding electrodes formed thereon, an electrode material containing photopolymerizable materials is printed on a semiconductor element package region on the circuit board such that a film is formed with a prescribed thickness, concave circuit electrodes are formed by baking the electrode material film after exposure and development are performed so as to allow the electrode material film to remain only on prescribed electrode regions, the concave circuit electrode having edges warped in a direction of going apart from a board surface, the protruding electrodes formed on the semiconductor element are brought into contact with the concave sides of the concave circuit electrodes, and the protruding electrodes and the circuit electrodes are connected with each other via the conductive resin.

Further, the present invention is characterized by forming the electrode material film with a dry film thickness of 10 to 20 micrometers by using a flip-chip packaging method.

Moreover, the present invention is characterized in that the electrode material film remaining after development is trapezoidal in cross section that is wider as it goes farther from the circuit board.

Also, the present invention is characterized in that the circuit electrode is arc-shaped in cross section according to the flip-chip packaging method.

Besides, according to the present invention, a flip-chip package, in which the semiconductor element having the protruding electrodes formed thereon is packaged on the circuit board by using the conductive resin, is characterized in that the circuit board includes the concave circuit electrodes each having edges warped in a direction of going apart from the board surface, the semiconductor element is disposed such that the ends of the protruding electrodes are

in contact with the concave surfaces of the concave circuit electrodes, and the protruding electrodes and the circuit electrodes are connected to each other via the conductive resin.

Furthermore, according to the present invention, the circuit board for flip-chip packaging the semiconductor element, which has the protruding electrodes formed thereon, by using the conductive resin, is characterized by including the concave circuit electrodes each having edges warped in a direction of going apart from the board surface.

Referring to drawings, the embodiments of the present invention will be discussed in a specific manner.

FIG. 1 is a process sectional view explaining a method of packaging a semiconductor element according to Embodiment 1 of the present invention.

As shown in FIG. 1(a), a paste electrode material 2 containing photopolymerizable materials is printed on an area for placing a semiconductor element on a circuit board 1. After printing, the electrode material 2 is dried at a suitable temperature without flowing. At this moment, the electrode material 2 is printed while a printing type and conditions are determined so as to have a film thickness of 10 to 20 μm after drying.

Then, as shown in FIG. 1(b), a glass mask 3 is disposed on the film of the electrode material 2 while being positioned on the circuit board 1. Openings 3a are formed on the glass mask 3 to transmit light through a desired circuit pattern. To be specific, the 50 μm-width openings 3a corresponding to electrode regions are formed with a 100 μm-pitch. Then, UV (ultraviolet ray) having a wavelength of 320 to 370 nm is radiated at 300 to 500 mJ from the above of the glass mask 3.

As shown in FIG. 1(c), due to UV passing through the openings 3a, photopolymerizable materials of the electrode material 2 on the electrode regions 2a, i.e., a photoinitiator,

a monomer, and a polymer are reacted with one another to proceed polymerization. In contrast, regarding photopolymerizable materials of the electrode material 2 on non-electrode regions 2b, polymerization does not occur. Since UV is not likely to enter the neighborhood of the circuit board 1, the electrode materials 2 are not likely to be polymerized on these regions.

Subsequently, the electrode material 2 is developed by using an alkaline solution and so on. Thus, it is possible to dissolve and remove the electrode material 2 on the non-electrode regions 2b having no polymerization or insufficient polymerization. As shown in FIG. 1(d), this operation removes the electrode material 2 on the non-electrode regions 2b. In the vicinity of the surface of the electrode material 2 on the electrode regions 2a, polymerization is proceeded completely. Hence, the electrode material 2 remains without any erosion so as to correspond in shape to the openings 3a of the glass mask 3. Meanwhile, regarding the electrode material 2 around the circuit board 1, polymerization is not completed over a wide region as compared with the neighborhood of the surface, resulting in erosion larger than the openings 3a. Consequently, the electrode material 2 on the electrode region 2a is trapezoidal in cross section.

Thereafter, since the circuit board 1 is baked at a temperature of sintering the electrode material 2, as shown in FIG. 1(e), the electrode material 2 on the circuit board 1 is baked as circuit electrodes 4. According to FIG. 1(e), since the electrode material 2 contracts upon baking, the edges of the circuit electrodes 4 are warped in a direction of going apart from the circuit board 1 (edge curl), and the circuit electrodes 4 are arc-shaped depressions in cross section.

Finally, as shown in FIG. 1(f), the semiconductor element 7, on which conductive resin 6 is transferred to protruding

electrodes 5, is accurately positioned to the circuit substrate 1 such that the protruding electrodes 5 and the circuit electrodes 4 are opposed to each other. A suitable load is applied to the semiconductor element 7, the protruding electrodes 5 and the circuit electrodes 4 are brought into contact with each other, and the conductive resin 6 is cured. Hence, the flip chip packaging of the semiconductor element 7 is completed.

In the flip chip package manufactured in the above manner, the edge-curled circuit electrodes 4 prevent the conductive resin 6 from being squeezed out of the circuit electrodes 4. Therefore, at the time of packaging the semiconductor element 7 with a 100-μm electrode pitch, the conductive resin 6 expanding laterally does not cause any short circuits between the adjacent electrodes.

Now, the circuit electrodes 4 will be further discussed.

As shown in FIG. 1(e), a maximum distance from the surface of the circuit board 1 to the edge-curled circuit electrodes 4 is defined as an edge curl amount L (see FIG. 1(e)). An edge curl amount L is considerably dependent upon a dry film thickness of the electrode material 2 shown in FIG. 1(a). When a dry film thickness is 10 to 20 μm, an edge curl amount L is 2 to 10 μm. Thus, the circuit electrodes 4 can act as saucers.

Meanwhile, when a dry film thickness is larger than 20 μm, parts not being polymerized on the circuit board 1 are larger in thickness, and the electrode material 2 to be developed and removed on the circuit board 1 remains, resulting in short circuits. In contrast, when a dry film thickness is 10 μm or less, an edge curl amount L is 2 μm or less and the circuit electrodes 4 cannot sufficiently act as saucers.

FIG. 2 is a process sectional view explaining a method of packaging a semiconductor element according to Embodiment 2 of the present invention.

As shown in FIG. 2(a), like Embodiment 1, edge-curled circuit electrodes 4 are formed on a circuit substrate 1. And then a mask (not shown) having openings corresponding to the circuit electrodes 4 is positioned onto the circuit electrodes 4, and conductive resin 6 is applied to the circuit electrodes 4 as shown in FIG. 2(b) by using a printing method and so on. Thereafter, as shown in FIG. 2(c), a semiconductor element 7 having protruding electrodes 5 formed thereon is positioned to the circuit board 1, and a suitable load is applied onto the semiconductor element 7. Hence, the flip chip packaging of the semiconductor element 7 is completed.

According to such a method as well, like Embodiment 1, the edge-curled circuit electrodes 4 act as saucers to prevent the conductive resin 6 from being squeezed out, thereby eliminating the occurrence of short circuits.

(Experimental Example)

A semiconductor element is packaged according to the above manufacturing steps and the performance is evaluated. Used members and materials are:

circuit board: low-temperature baked ceramic multilayered board (test pattern)

board size: 30 × 30 × 0.65 (mm)

electrode pitch: 100 (μm)

number of electrodes: 360 pins

The electrode material 2 contains Ag as a metallic component with a dry film thickness of about 15 μm. And then, the electrode material film is exposed and developed using a glass mask having openings formed thereon. The openings are each about 50 μm in width. The electrode material 2 on the non-electrode regions 2b having no or insufficient polymerization is dissolved and removed. The circuit board 1, on which the electrode material 2 on the non-electrode regions 2b is dissolved and removed, is baked at about 800 to 1000°C. Hence, the electrode material 2 on the circuit board 1 is baked as circuit electrodes 4. At this moment,

an edge curl amount L is 4 μm. Ni plating and Au plating are applied to protect the surface.

IC: dummy IC

IC size 10 × 10 × 0.5 (mm)

IC electrode pad pitch: 100 (μm)

Number of pins: 360 pins

The protruding electrodes 5 are formed on the electrodes of the above IC by using metallic wires, and the conductive resin 6 is transferred onto the formed protruding electrodes 5. The conductive resin 6 contains Ag as a metallic component and epoxy as a resin component. The IC including the conductive resin 6 is positioned onto the circuit board 1 and a weight of several grams is applied to each of the protruding electrodes so as to complete packaging. And then, after curing the conductive resin 6 by heating, evaluation is made on short/open. FIG. 1 shows the result.

Table 1

Method of Present Invention	Open	0/5 Package
	Short	0/5 Package
Conventional Method	Open	0/5 Package
	Short	4/5 Package

As understood from Table 1, the method of the present invention does not cause any opens or short circuits at all. Meanwhile, the conventional method causes short circuits on a 4/5 package. Thus, the effectiveness of the present invention can be confirmed.

As described above, according to the present invention, the edge-curled circuit electrodes are formed on the circuit board, and the protruding electrodes of the semiconductor element are connected to the circuit electrodes by using the conductive resin. Hence, it is possible to prevent the conductive resin from being squeezed out while the circuit electrodes act as saucers, achieving a reliable packaging for

the semiconductor element without any occurrence of short circuits.

CLAIMS

1. A flip-chip packaging method, wherein

in flip-chip packaging a semiconductor element on a circuit board by using conductive resin, said element having protruding electrodes formed thereon, the method comprising:

printing an electrode material containing photopolymerizable materials on a semiconductor element package region on said circuit board such that a film is formed with a prescribed thickness, and forming concave circuit electrodes by baking said electrode material film after performing exposure and development of said electrode material film to allow said electrode material film to remain only on prescribed electrode regions, thereby forming concave circuit electrodes having edges warped in a direction of going apart from the circuit board surface; and

bringing said protruding electrodes formed on said semiconductor element into abutment with concave faces of said concave circuit electrodes, and connecting said protruding electrodes and said circuit electrodes with each other via the conductive resin.

2. The flip-chip packaging method according to claim 1, wherein said electrode material film is formed to have a dry film thickness of 10 to 20 micrometers.

3. The flip-chip packaging method according to claim 1 or 2, wherein said electrode material film remaining after development is trapezoidal in cross section that is wider as it goes farther away from said circuit board.

4. The flip-chip packaging method according to claim 1 or 2, wherein said circuit electrode is arc-shaped in cross section.

5. A flip-chip package in which a semiconductor element having protruding electrodes formed thereon is packaged on a circuit board by using conductive resin, wherein

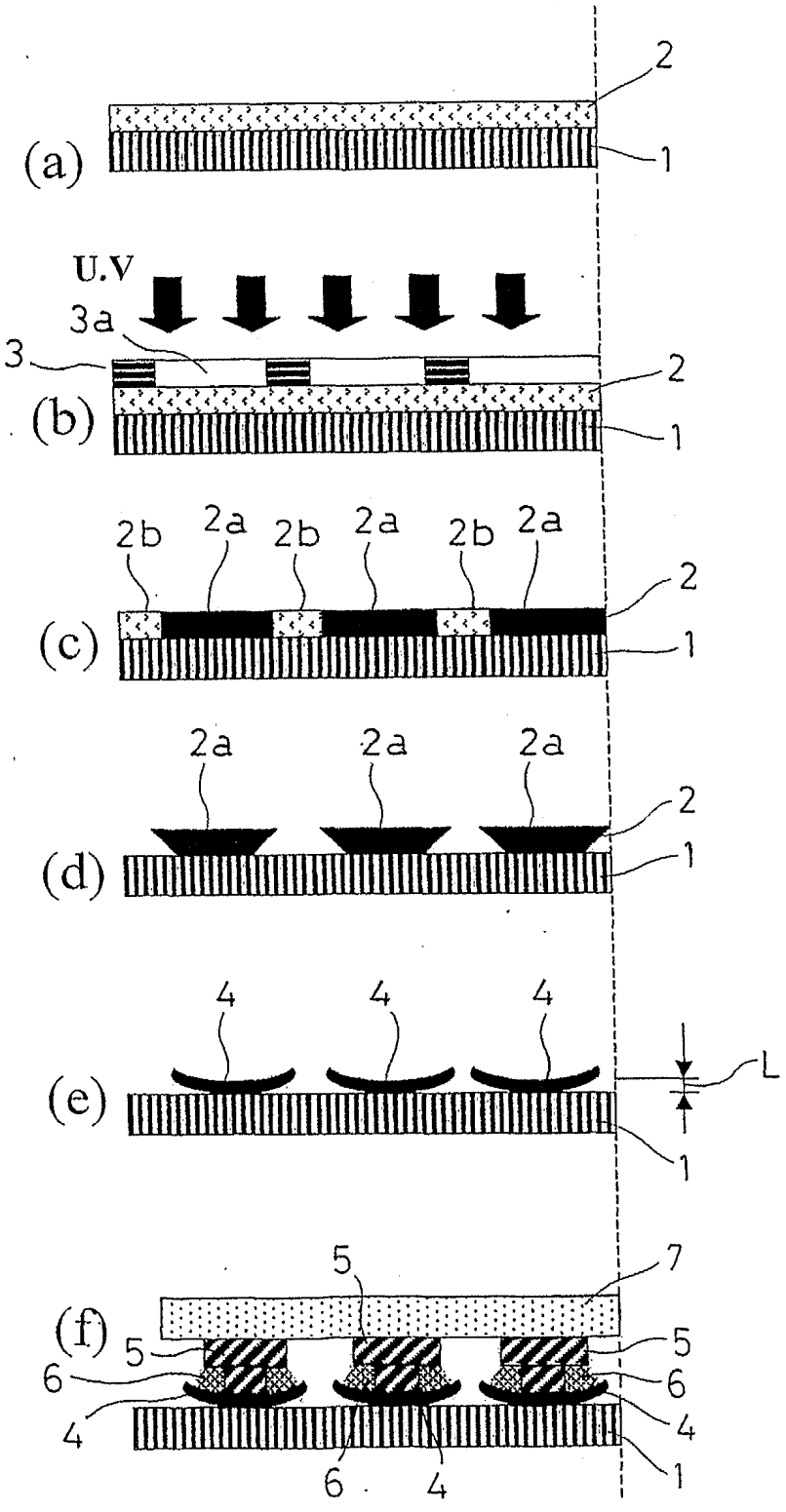
said circuit board includes concave circuit electrodes each having edges warped in a direction of going apart from the circuit board surface,

said semiconductor element is disposed such that ends of said protruding electrodes thereof come in abutment with concave surfaces of said concave circuit electrodes, and

said protruding electrodes and said circuit electrodes are connected to each other via the conductive resin.

6. A circuit board for flip-chip packaging a semiconductor element by using conductive resin, said element having protruding electrodes formed thereon, comprising concave circuit electrodes each having edges warped in a direction of going apart from the circuit board surface.

FIG. 1


(a)
2
1
U.V
3a
3
(b)
2
1
2b
2a
2b
2a
2b
2a
(c)
2
1
2a
2a
2a
(d)
2
1
4
4
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5
7
(f)
5
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4
6
4
1

FIG. 2

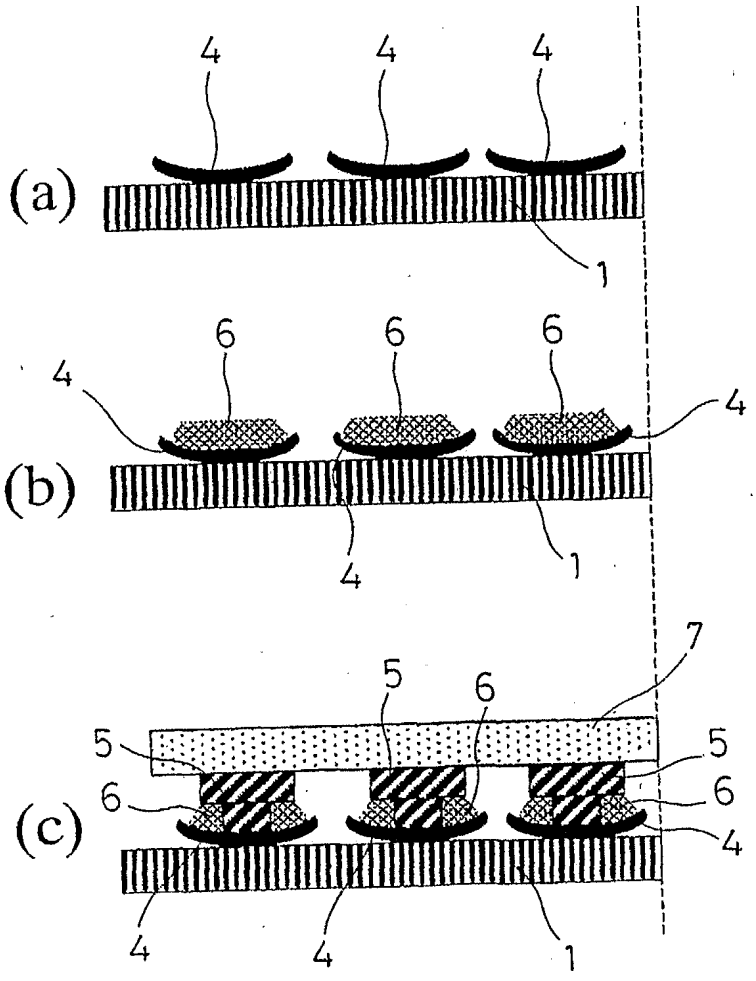
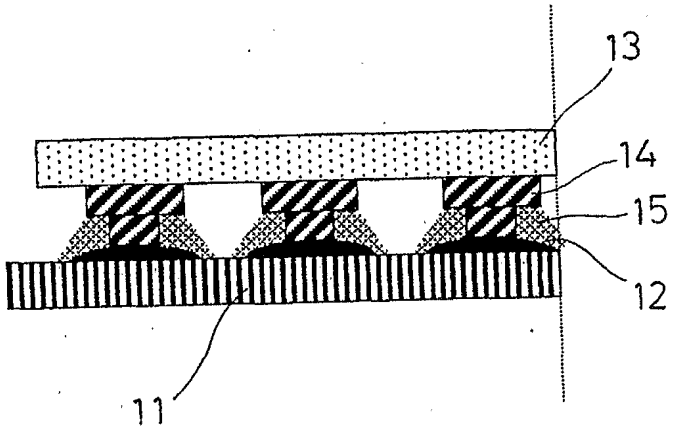


FIG. 3



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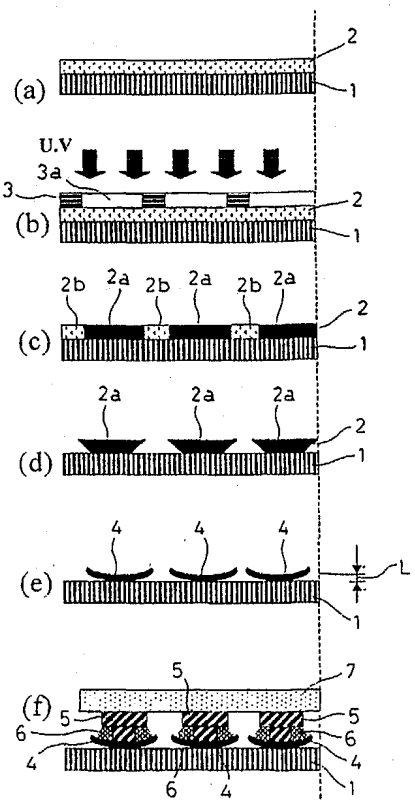
(54) Title: FLIP CHIP PACKAGE, CIRCUIT BOARD THEREOF AND PACKAGING METHOD THEREOF



(57) Abstract: According to the present invention, when a semiconductor element having protruding electrodes formed thereon is connected to a circuit board via conductive resin, stable connection is made even when an electrode pitch is small on the semiconductor element. On semiconductor element package regions on the circuit board, a paste electrode material containing photopolymerizable materials is printed to form a film having a prescribed thickness, and this electrode material film is baked after exposure and development thereof so as to obtain circuit electrodes having edges warped in a direction of going apart from the circuit board surface. Then, the protruding electrodes and the concave surfaces of the circuit electrodes are brought in abutment with each other and connected via the conductive resin which surrounds the abutments between the respective electrodes and is held on the concave surfaces of the circuit electrodes. With this arrangement, the concave surfaces of the circuit electrodes act as saucers and prevent the conductive resin from being squeezed out, thereby eliminating possible occurrence of short circuits.

WO 02/09485 A2

PCT3144

PCT REQUEST

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0	**For receiving Office use only**	
0-1	International Application No.	
0-2	International Filing Date	
0-3	Name of receiving Office and "PCT International Application"	

0-4	**Form - PCT/RO/101 PCT Request**	
0-4-1	Prepared using	PCT-EASY Version 2.92 (updated 01.03.2001)
0-5	**Petition**	
	The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Japan Patent Office (RO/JP)
0-7	**Applicant's or agent's file reference**	PCT3144
I	**Title of invention**	FLIP CHIP PACKAGE, CIRCUIT BOARD THEREOF AND PACKAGING METHOD THEREOF
II	**Applicant**	
II-1	This person is:	applicant only
II-2	Applicant for	all designated States except US
II-4	Name	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
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II-7	State of residence	JP
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II-9	Facsimile No.	06-6906-1643
III-1	**Applicant and/or inventor**	
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III-1-7	State of residence	JP

PCT REQUEST

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III-2	**Applicant and/or inventor**	
III-2-1	This person is:	applicant and inventor
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III-2-6	State of nationality	JP
III-2-7	State of residence	JP
IV-1	**Agent or common representative; or address for correspondence** The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
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IV-1-3	Telephone No.	06-6532-4025
IV-1-4	Facsimile No.	06-6543-2205
V	**Designation of States**	
V-1	Regional Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	EP: AT BE CH&LI CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR and any other State which is a Contracting State of the European Patent Convention and of the PCT
V-2	National Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	CN ID KR SG US
V-5	**Precautionary Designation Statement** In addition to the designations made under items V-1, V-2 and V-3, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) of the State(s) indicated under item V-6 below. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit.	
V-6	**Exclusion(s) from precautionary designations**	NONE

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VI-1	**Priority claim of earlier national application**		
VI-1-1	Filing date	21 July 2000 (21.07.2000)	
VI-1-2	Number	Patent Application 2000-219911	
VI-1-3	Country	JP	
VI-2	**Priority document request**		
	The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s):	VI-1	
VII-1	**International Searching Authority Chosen**	European Patent Office (EPO) (ISA/EP)	
VIII	**Declarations**	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	-	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	-	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	-	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	-	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	-	
IX	**Check list**	number of sheets	electronic file(s) attached
IX-1	Request (including declaration sheets)	4	-
IX-2	Description	12	-
IX-3	Claims	2	-
IX-4	Abstract	1	EZABST00.TXT
IX-5	Drawings	3	-
IX-7	TOTAL	22	
	Accompanying items	paper document(s) attached	electronic file(s) attached
IX-8	Fee calculation sheet	✓	-
IX-9	Original separate power of attorney	✓	-
IX-17	PCT-EASY diskette	-	Diskette
IX-18	Other (specified):	Sheets pasted with revenue stamps each for Transmittal fee and for Priority document fee	-
IX-18	Other (specified):	Sheets pasted with bank drafts each for Search fee and for International fee	-

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IX-19	**Figure of the drawings which should accompany the abstract**	1
IX-20	***Language of filing of the international application***	English
X-1	**Signature of applicant, agent or common representative**	
X-1-1	Name (LAST, First)	MORIMOTO, Yoshihiro

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10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported *international application***	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/EP
10-6	**Transmittal of search copy delayed until search fee is paid**	

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(71) Applicant: **MATSUSHITA ELECTRIC IND CO LTD**

(72) Inventor: **BESSHO YOSHIHIRO**

(54) MOUNTING OF SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: To electrically connect a semiconductor device to a circuit board with good reliability by a method wherein a convex bump electrode composed of a two-step shape of a pedestal part and a top part is installed on an electrode pad part of the semiconductor device and the bump electrode is connected electrically to a terminal electrode part on the circuit board via a conductive adhesive having flexibility.

CONSTITUTION: When a semiconductor device 1 is mounted on a terminal electrode part 5 on a circuit board 6, a convex bump electrode 3 composed of a two-step shape of a pedestal part and a top part is formed on an electrode pad part 2 of the semiconductor device 1; the bump electrode 3 is connected electrically to the terminal electrode part 5 on the circuit board 6 via a conductive adhesive 4 having flexibility. For example, a two-step-shaped and projected bump electrode 3 is formed in advance on an electrode pad part 2 of a semiconductor device 1 ; a conductive adhesive 4 having flexibility is formed on the bump electrode 3 by a transcription operation or a printing operation. After that, the semiconductor device 1 is aligned with a terminal electrode part 5 of a circuit board 6 in a face-down manner, the semiconductor device 1 is mounted on the circuit board 6; after that, the conductive adhesive 4 is hardened by heating.